ABSTRACT OF THE DISCLOSURE

The present digital synchronous circuit includes a clock generating circuit for outputting a plurality of clock signals CLK1 to CLKn, a plurality of first latch circuits, each for receiving an input data signal DIN at a data input terminal and for receiving a corresponding clock signal at a clock input terminal, a plurality of second latch circuits, each for latching, in response to the receipt of a control signal LC, an output signal from a corresponding first latch circuit, and a control circuit for receiving input data signal DIN to generate control signal LC. Control circuit outputs control signal LC after a delay of a prescribed period of time after the change in input data signal DIN. As a result, the adverse influence of the meta-stable state that occurs when sampling an asynchronous input data signal DIN is avoided, while at the same time, the chip size and power consumption are limited.